

HIGH-VOLTAGE MIXED-SIGNAL IC

UC1608

128x240 Matrix LCD Controller-Driver

Product Specifications
Revision 1.0

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ULTRACHIP

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UC1608

Single-Chip, Ultra-Low Power Passive Matrix LCD Controller-Driver

INTRODUCTION

UC1608 is an advanced high-voltage mixed-signal CMOS IC, especially designed for the display needs of ultra-low power hand-held devices.

In addition to low power column and row drivers, these ICs contain all necessary circuits for high-V LCD power supply, bias voltage generation, timing generation and graphics data memory.

Advanced circuit design techniques are employed to minimize external component counts and reduce connector size while achieving extremely low power consumption.

MAIN APPLICATIONS

- Cellular Phones, Smart Phones, and other battery operated palm top devices and/or portable Instruments

FEATURE HIGHLIGHTS

- Single chip controller-driver with built-in display RAM to support up to 128 x 240 dot matrix graphics LCD
- Ultra-low power consumption under all display patterns.

- Single-chip LCD controller-driver with built-in display data RAM and display timing generator.
- Crosstalk suppression circuit architecture for optimum image quality.
- Two selectable multiplexing rates: 128, 96.
- Wide supply voltage range: 2.4V ~ 3.5V
- 4 temperature compensation coefficients.
- Support 8/4 -bit high speed parallel interface.
- Built-in oscillators, V_{LCD} booster and serial interface to support compact LCD module connectors.
- Built-in charge pump allows the use of low V_{DD} while produces high enough V_{LCD} for driving LCD.
- Self-configuring on-chip V_{LCD} generator with on-chip pumping capacitor requires only 5 external capacitors.
- Flexible data addressing/mapping schemes to support wide ranges of software models and LCD layout placements.
- On-chip bias generator supports flexible fine adjustments of LCD driving voltages to achieve optimum image quality while using minimum power.

	LCD	V_{DD}	V_{LCD}	Condition	I_{DD}	Power
UC1608	128 x 240	3.0V	13.6V	Note 1	330 μ A	990 μ W
		2.4V	13.6V	Note 1	370 μ A	888 μ W

Note 1 LCD drivers active, internally generated V_{LCD} , loaded with LCD pixel = $((0.205+0.015) \text{ mm})^2$.
Display Pattern: 25% checker, 25% ON, 50% OFF.

ORDERING INFORMATION

Nomenclature	Description
UC1608-I-P-A-V	I: Interface I->I2C Bus X-> non I2C Bus P: Package P->TCP, G->Au Bumped Die, F->COF A: A-> STD version, B-Z->customized version V: version control

Part Number	Memory	Drivers	Mux Rate Supported	Versions
UC1608XGAC	128 x 240	128R x 240C	1/128, 1/96	
UC1608XTAC	128 x 240	128R x 240C	1/128, 1/96	

General Notes**APPLICATION INFORMATION**

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

BARE DIE DISCLAIMER

All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing for a period of ninety (90) days from the date of UltraChip's delivery. There is no post wafer saw/pack testing performed on individual die. Although the latest modern processes are utilized for wafer sawing and die pick-&-place into waffle pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and qualify their application in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

LIFE SUPPORT APPLICATIONS

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

PIN DESCRIPTION

Name	Type	Chip Pads	TCP Pins	Description
Main Power Supply				
V _{DD1} , V _{DD2} , V _{DD3}	PWR	325, 326, 327	391, 392, 392	V _{DD1} supplies for display data RAM and digital logic, V _{DD2} supplies for V _{LCD} /V _B generator, V _{DD3} supplies for V _{REF} and other analog circuits. V _{DD2} /V _{DD3} should be connected to the same power source. But V _{DD1} can be connected to a source voltage no higher than V _{DD2} /V _{DD3} .
V _{SS} V _{SS2}	GND	329, 328	393	Ground. Connect V _{SS} and V _{SS2} to the shared GND pin.
LCD Power Supply				
V _{B3+} V _{B3-} V _{B2+} V _{B2-} V _{B1+} V _{B1-} V _{B0+} V _{B0-}	PWR	348,350 344,346 340,342 336,338	401,402 399,400 397,398 395,396	LCD Bias Voltages. These voltages are always generated internally. Connect capacitors of C _B value between V _{BX+} to V _{BX-} .
V _{S3+} V _{S3-} V _{S2+} V _{S2-} V _{S1+} V _{S1-} V _{S0+} V _{S0-}	PWR	349,351 345,347 341,343 337,339	401,402 399,400 397,398 395,396	The sense pins for C _B capacitors. These pins are wired together with V _B pins in TCP package.
V _{LCD-IN} V _{LCD-OUT}	PWR	334 333	394	Main LCD Power Supply. When internal V _{LCD} is used, connect these pins together. When external V _{LCD} source is used, connect external V _{LCD} source to V _{LCD-IN} pins and leave V _{LCD-OUT} open. A by-pass capacitor C _L should be connected between V _{LCD} and V _{SS} .
Test Pins				
TP [2:0]	I	332~330		Test programming. Leave these pins open.
TST	I	312	377	Test pin. In normal operation, connect this pin to ground.
TST[2:0]	I/O	307,318,308		Test pins. In normal operation, leave these pins open.

NOTE

- Recommended capacitor values:
C_B: 30x ~ 50x LCD load capacitance or 1uF (3V), whichever is higher.
C_L: 50x ~ 80x LCD load capacitance or 1uF (20V), whichever is higher.
- Ceramic capacitors are recommended for C_B and C_L.

Name	Type	Chip Pads	TCP Pins	Description
HOST INTERFACE				
PS1 PS0	I	309, 310	374, 375	Bus modes: 8 bits Parallel modes: "HL" : 8080 "HH" : 6800 4 bits Parallel modes : "LL" : 8080 "LH" : 6800
CE	I	311	376	Chip Select. Chip selected when CE="H".
RST	I	313	377	When RST="L", all control registers are re-initialized by their default states and/or by their pin configurations if applicable. When RST is not used, connect the pin to V _{DD1} .
CD	I	314	378	Select Control data or Display data for read/write operation. "L": Control data "H": Display data
WR0 WR1	I	315 316	379 380	WR[1:0] controls the read/write operation of the host interface. WR[1:0] meaning depends on whether the interface is in the 6800 mode or the 8080 mode.
D0~D7	I/O	317 ~ 324	381 ~ 388	Bi-directional parallel host interface
LCD DRIVE OUTPUT				
SEG1,~ SEG240	HV	1 ~ 240	67 ~ 306	LCD column driver outputs. Support up to 240 columns. Leave unused drivers open-circuit.
COM1, COM3, ..COM127 COM2, COM4, ... COM128	HV	242~260, 262~306 416~398, 396~352	307~370 62, ~ 3	LCD row driver outputs. Support up to 128 rows. Drivers for even and odd row are group into two separate groups along the two sides of the IC. Leave unused drivers open-circuit.

NOTE

- Unless otherwise specified, connect all unused input pins and control pins to V_{SS}.

CONTROL REGISTERS

UC1608 contains registers which controls the chip operation. These registers can be modified by commands. The commands supported by UC1608 are described in the next section.

Name: The Symbolic reference of the register byte.
Note that, some symbol names refers to collection of bits (flags) within one register byte.

Default: Value after *Power-up-Reset* and *System-Reset*.
"PIN" means default value depends on the connection of associated configuration pin(s).

Name	Bits	Default	Description
SL	6	0H	Start Line. Mapping from Row0 to Display Data RAM.
CR	8	0H	Return Column Address.
CA	8	0H	Display Data RAM Column Address (Used in Host to Display Data RAM access)
PA	4	0H	Display Data RAM Page Address (Used in Host to Display Data RAM access)
BR	2	2H	Bias Ratio.
TC	2	0H	Temperature Compensation.
GN	2	3H	Gain, V_B / V_{PM}
MR	1	1H	Multiplexing Rate: Number of pixel rows: 0: 96 1: 128
PM	6	0H	Electronic Potential Meter to fine tune V_{PM} in reference to V_{REF}
OM	2	0	Operating Modes 10: Sleep 11: Normal 01: (Not used) 00: Reset
BZ	1	–	BZ: Busy with internal processes (reset, changing mode, etc.) Use only Display RAM read/write access.
RS	1	–	RS: Reset in progress, Host Interface not ready
PC	3	07H	V_{LCD} Pump Control. PC[0]: 1: Regular LCD load 0: Low LCD load PC[2:1]: 00: External V_{LCD} , 01: 6x 10: 7x 11: 8x
APC0	8	00H	Advanced Program Control. Consult UltraChip application engineering department for details.

Name	Bits	Default	Description
DC	5	0H	Display Control: DC[0]: PXV: Pixels Inverse DC[1]: APO: All Pixels ON DC[2]: Display Enable
AC	4	0H	Address Control: AC[0]: WA: Automatic column/page Wrap Around AC[1]: when set 1, page address is first. AC[2]: PID: PA (page address) auto increment direction (L:+1 H:-1) AC[3]: CUM: Cursor update mode, when CUM=1, CA increment on write only, wrap around suspended
LC	4	0 0 0 0	LCD Layout Control: LC[0]: MSF: MSB First mapping Option LC[1]: Reserved (always set to 0) LC[2]: MX, Mirror X (Column sequence inversion) LC[3]: MY, Mirror Y (Row sequence inversion)

COMMANDS

The following is a list of host commands support by UC1608

- C/D: 0: Control, 1: Data
 W/R: 0: Write Cycle, 1: Read Cycle
 # Useful Data bits
 – Don't Care

Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action
Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte @ PA/CA
Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte @ PA/CA
Get Status	0	1	BZ	MX	DE	RS	WA	GN1	GN0	1	Get Status Summary
Set Column Address LSB	0	0	0	0	0	0	#	#	#	#	Set CA[3:0]=D[3:0]
Set Column Address MSB	0	0	0	0	0	1	#	#	#	#	Set CA[7:4]=D[3:0]
Set Mux rate & Temperature Compensation.)	0	0	0	0	1	0	0	#	#	#	Set MR=D[2] Set TC[1:0]=D[1:0]
Set Power Control	0	0	0	0	1	0	1	#	#	#	Set PC[2:0]=D[2:0]
Set Adv. Program Control (double byte command)	0	0	0	0	1	1	0	0	R		Set APC[R][7:0]=D[7:0], where R = 00, or 01
Set Start Line	0	0	0	1	#	#	#	#	#	#	Set SL[5:0]=D[5:0]
Set V _{REF} potential meter (double-byte command)	0	0	1	0	0	0	0	0	0	1	Set PM[5:0]=D[5:0] Set GN:0]=D[7:6]
Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]=D[2:0]
Set Column Mirroring	0	0	1	0	1	0	0	0	0	#	Set LC[2]=D0
Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]=D0
Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]=D0
Set Display ON/OFF	0	0	1	0	1	0	1	#	#	#	Set DC[4:2]=D[2:0]
Set Page Address	0	0	1	0	1	1	#	#	#	#	Set PA[3:0]=D[3:0]
Set LCD to RAM Mapping	0	0	1	1	0	0	#	#	#	#	Set LC[3:0]=D[3:0]
System Reset	0	0	1	1	1	0	0	0	1	0	System Reset sequence
NOP	0	0	1	1	1	0	0	0	1	1	No operation
Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]= D[1:0]
Reset Cursor Update Mode	0	0	1	1	1	0	1	1	1	0	Set AC[3]=0, CA=CR;
Set Cursor Update Mode	0	0	1	1	1	0	1	1	1	1	Set AC[3]=1, CR=CA;
Set Test Control (double byte command)	0	0	1	1	1	0	0	1	TT		For testing only. Do not use.
	0	0	#	#	#	#	#	#	#	#	

NOTE:

Other than commands listed above, all other bit patterns result in NOP (No Operation).

LCD VOLTAGE SETTING

MULTIPLEX RATES

The common scanning pulse's multiplex rate is determined by a software programmable register MR. Two multiplex rates are supported by UC1608: 96, 128.

BIAS SELECTION

Bias Ratio (BR) is defined as the ratio between V_{LCD} and V_B , i.e. $BR = V_{LCD}/V_B$, where V_B is the voltage difference between the segment electrodes and non-scanned common electrodes. Mathematically, $V_B = V_{B1+} - V_{B1-} = V_{B0+} - V_{B0-}$.

The optimum *Bias Ratio* is estimated as:

$$\sqrt{Mux} + 1$$

UC1608 supports four bias ratios (BR) as listed below. BR can be selected via software program.

BR	0	1	2	3
Bias Ratio	10.67	11.33	12	12.67

Table 2: Bias Ratios

V_B GENERATION

V_B is generated internally by UC1608. The value of V_B is determined by three control registers: GN (Gain), PM (Potential Meter), TC (Temperature Compensation) with the following relationship:

$$V_B = Gain \times V_{PM}$$

where V_{PM} is the output of an on-chip electronic potential meter. The value of V_{PM} is given by:

$$V_{PM} = \frac{600 + PM}{1200} \times V_{REF}$$

The value of *Gain* is controlled by $GN[2:0]$, as shown in the table below:

$GN[1:0]$	00	01	10	11
Gain	1.66	1.82	2.00	2.20

Table 3: Gain vs. GN value

V_{REF} TEMPERATURE COMPENSATION

V_{REF} is a temperature compensated reference voltage. V_{REF} increases automatically as ambient temperature cools down. The temperature compensation coefficients are given in the following table:

TC	0	1	2	3
% per °C	0.0	-0.05	-0.10	-0.20

Table 4: Temperature Compensation

For all TC values, V_{REF} are normalized to 1.25V at 25 °C. When selecting TC , make sure V_{B+} and V_{LCD} stays within specified UC1608 ratings across entire operating temperature range.

V_{LCD} SELECTION

V_{LCD} may be supplied either by internal charge pump or by external power supply. The source of V_{LCD} is determined by registers $PC[2:1]$.

When V_{LCD} is generated internally its value has the following relationship with V_B :

$$V_{LCD} = BiasRatio \times V_B$$

Given $V_{REF} = 1.25V$ at 25 °C, V_{LCD} becomes:

$$V_{LCD} \cong BiasRatio \times Gain \times \frac{600 + PM}{1200} \times 1.25 \quad (1)$$

When $PM = 0$, then equation (1) becomes:

$$V_{LCD} \cong BiasRatio \times Gain / 1.6 \quad (1b)$$

LOAD DRIVING STRENGTH

UC1608's drivers and power supply circuits are designed to handle capacitance load of >1pF per pixel when $V_{DD} > 2.4V$.

POWER SUPPLY CONFIGURATION

UC1608 has a built-in charge pump with on-chip pumping capacitors. The number of pump stages used can be programmed by setting $PC[2:1]$ register. Make sure the chip is in Reset mode before changing the value of PC .

Given the same display quality, the lower the PC setting the more efficient UC1608's charge pump will be, but the weaker is the driving strength. System designers are recommended to verify the design with the highest setting first before lower PC settings to achieve better efficiency.

Due to the use of fully embedded power supply, built-in power ready detector, and draining circuit, there is no rigid power up, power down sequences for UC1608 controllers when using internal V_{LCD} generator.

On the other hand, caution must be exercised when external V_{LCD} source is used. The general rule of thumb is to make sure Display Enable is OFF before connecting or disconnecting external V_{LCD} sources.

LCD DISPLAY CONTROLS

CLOCK & TIMING GENERATOR

The built-in system clock of UC1608 is running at 335kHz. All required components for the clock oscillator are built-in. No external parts are required.

Row electrodes are scanned at a fixed rate of *System Clock / 32*

The resulting field rate is *Row rate / Multiplexing rate*.

DRIVER MODES

Row and column drivers can be in either Idle mode or Active mode, controlled by Display Enable flag (DC[2]). When column drivers are in idle mode, their outputs are high-impedance (open circuit). When row drivers are in idle mode, their outputs are connected to V_{SS}.

DRIVER ARRANGEMENTS

The naming conventions are: COM_x (where x=1~128) refers to the row driver for the x-th row of pixels on the LCD panel.

Row drivers are clustered into “even row drivers” and “odd row drivers”, along the two sides of the chip to enhance the symmetry of ITO layout.

The mapping of COM_x to LCD pixel rows is the same for all MR settings. When MR setting is 0, leave unused row drivers open.

LAYOUT CONSIDERATIONS FOR ROW ITO

Since UC1608 line rate is as fast as 100KHz and the row scanning pulse is only 100uS wide, it is critical to minimize the RC delay experienced by row electrodes.

It is recommended to optimize the ITO layout to limit the worst case row electrode RC delay as calculated below:

$$(R_{ROW}/2 + R_{ROUTE} + R_{OUT}) \times C_{ROW} < 2\mu S$$

where

- R_{ROW}: ITO resistance per row electrode within the matrix area
- R_{ROUTE}: ITO resistance leading from TCP to matrix area
- R_{OUT}: UC1608 output, 2K Ohm typical
- C_{ROW}: LCD loading capacitance of one row of pixels

DISPLAY CONTROLS

There are three groups of display control flags in the control register DC: Driver Enable (DE), All-Pixel-ON (APO) and Inverse (PXV). DE has the overriding effect over PXV and APO.

DRIVER ENABLE (DE)

Driver Enable is controlled by the value of DC[2] via *Set Display ON* command. DC[2] controls column drivers SEG1~240. When DC[2] is set, these column drivers are active. When DC[2] is reset, column drivers are set to high-impedance states.

ALL PIXELS ON (APO)

When set, this flag will force all active column drivers to output On signals, disregarding the data stored in the display buffer.

This flag has no effect when Display Enable is OFF and it has no effect on data stored in RAM.

INVERSE (PXV)

When this flag set to ON, active column drivers will output the inverse of the value it received from the display buffer RAM. This flag has no impact on data stored in RAM.

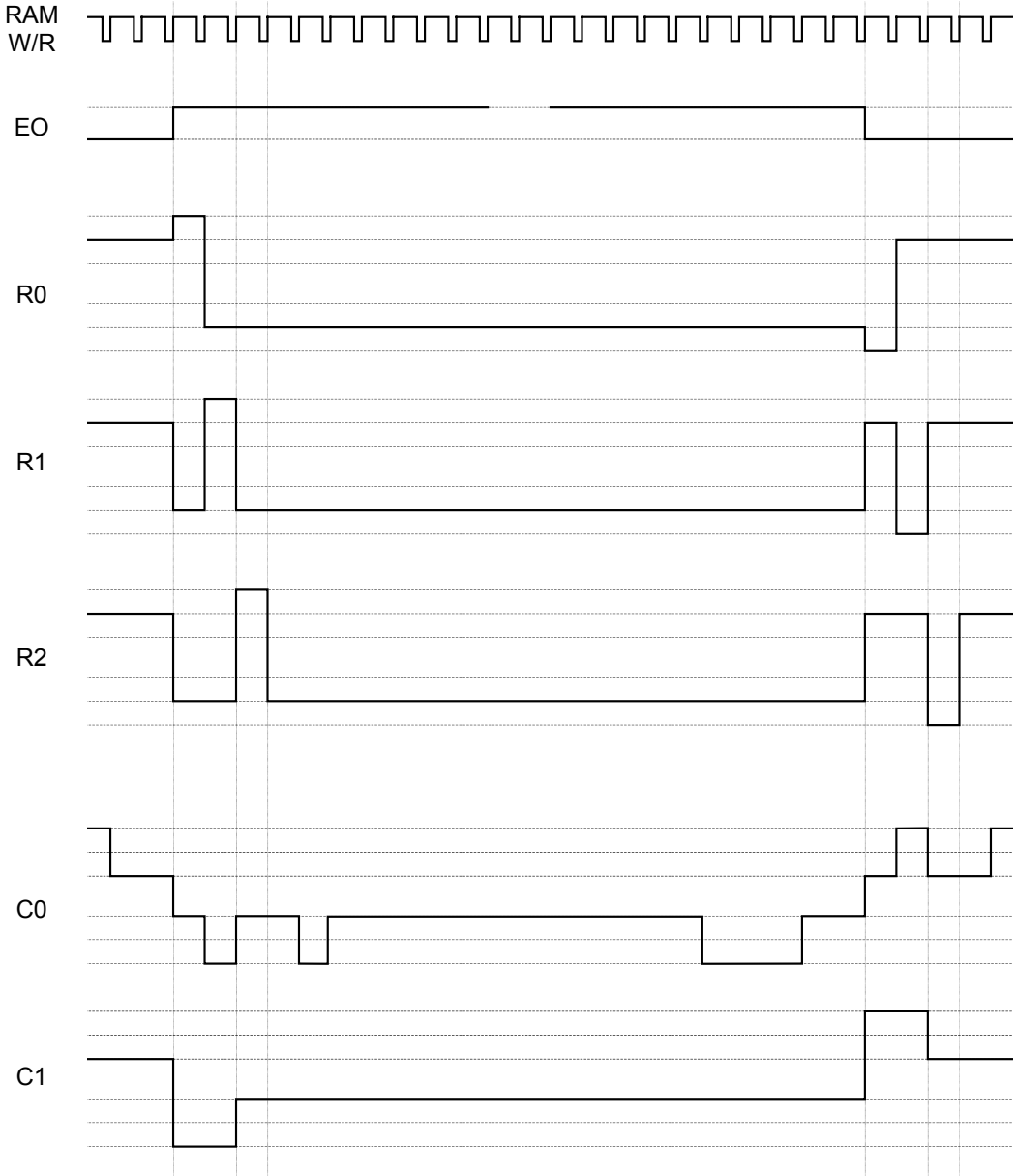


Fig. 4 Column and Row Driving Waveform

HOST INTERFACE

UC1608 series supports both 8/4 -bit parallel host interface formats.

Bus	Bus Type	Access
Parallel	8080	R/W
	6800	R/W

Table 5: Host interfaces Choices

actions are shown in the figure below. The generation of UC1608 internal bus control signals WR and RD is shown in the table below.

Bus Type	\overline{WR}	\overline{RD}
8080	WR0	WR1
6800	!(WR1 & !WR0)	!(WR1 & WR0)

Table 7: WR and RD signal generation

PARALLEL INTERFACE

It is possible to interface UC1608 controllers directly to either an 8080-style MPU bus or a 6800-style MCU bus with the following connection.

Bus Type	WR0	WR1
8080	\overline{WR}	\overline{RD}
6800	R/\overline{W}	E

Table 6: MPU bus control signal interface

The timing relationship between UC1608 internal control signal RD, WR and their associated bus

PARALLEL DATA TRANSFER

UC1608 Display Data RAM (RAM) read interface is implemented as a two-stage pipe-line. This architecture requires that, every time the bus interface switches from write to read, a dummy read cycle need to be inserted before the actual data can propagate through the pipe-line and be read from data port D[7:0].

There is no pipeline in write interface of RAM, and the data is transferred directly from data bus buffer to RAM.

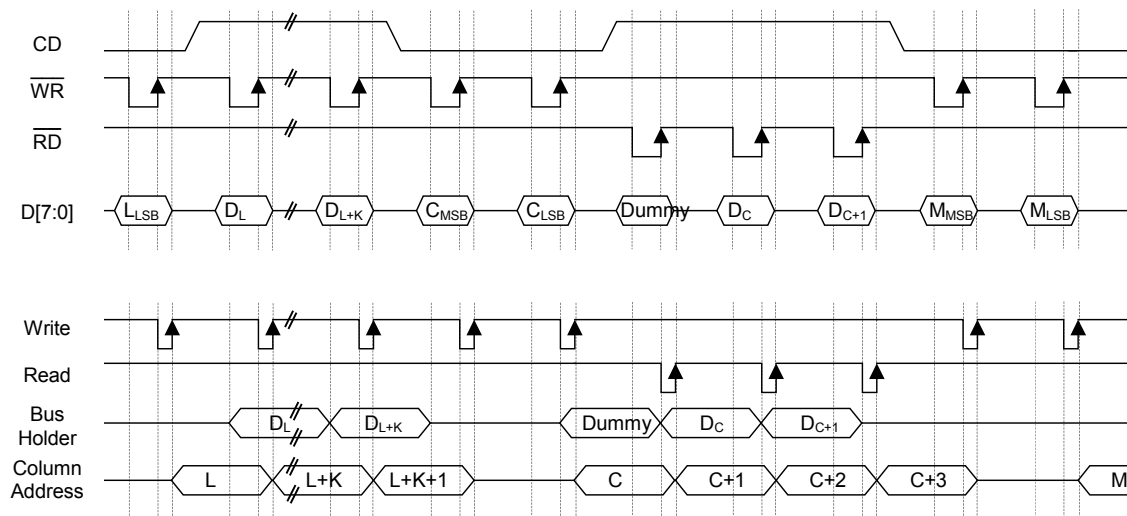


Figure 5: 8 bits Parallel Interface & Related Internal Signals

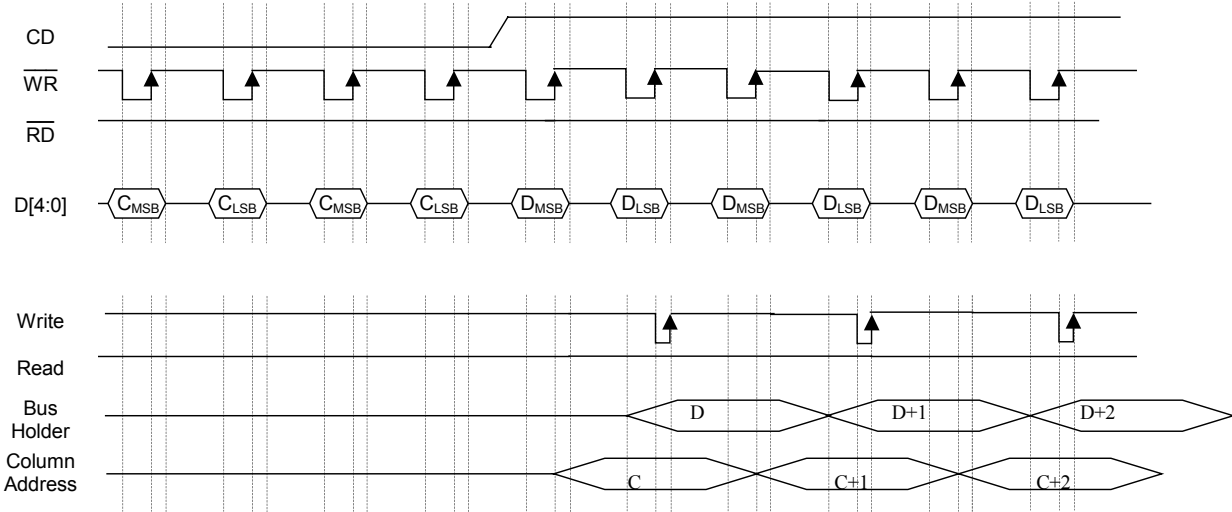


Figure 6 4bit Parallel Write Interface & Related Internal Signals

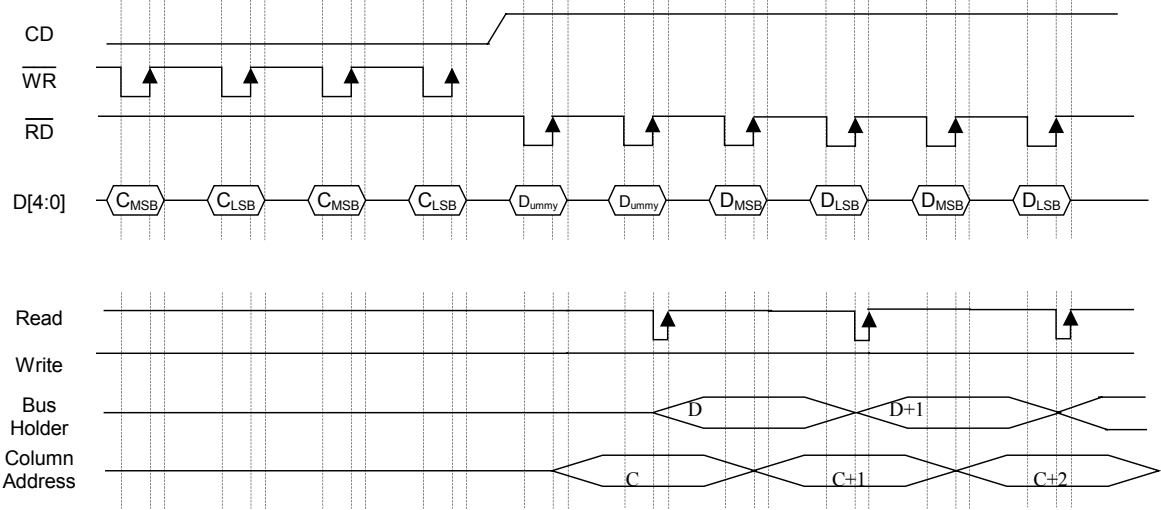


Figure 7: 4 bit Parallel Read Interface & Related Internal Signals

DISPLAY DATA RAM

DATA ORGANIZATION

The display data is one bit per pixel and stored in a dual port static RAM (RAM, for Display Data RAM). The RAM size is 128x240 for UC1608. This array of data bits are further organized into pages of 8 bit slices to facilitate parallel bus interface.

When Mirror X (MX, LC[2]) is OFF, the 1st column of LCD pixels will correspond to the bits of the first byte of each page, the 2nd column of LCD pixels correspond to the bits of the second byte of each page, etc.

MSB FIRST OR LSB FIRST

There are two options to map D[7:0] to RAM, MSB first (MSF=1), or LSB first (MSF=0), as illustrated below.

DISPLAY DATA RAM ACCESS

The memory used in UC1608 Display Data RAM (RAM) is a special purpose dual port RAM which allows asynchronous access to both its column and row data. Thus, RAM can be independently accessed both for Host Interface and for display operations.

DISPLAY DATA RAM ADDRESSING

A Host Interface (HI) memory access operation starts with specifying Page Address (PA) and Column Address (CA) by issuing *Set Page Address* and *Set Column Address* commands.

If wrap-around (WA, AC[0]) is OFF (0), CA will stop incrementing after reaching the end of page (240), and system programmers need to set the values of PA and CA explicitly.

If WA is ON (1), when CA reaches end of page, CA will be reset to 0 and PA will increment or decrement, depending on the setting of Page Increment Direction (PID, AC[2]). When PA reaches the boundary of RAM (i.e. PA = 0 or 15), PA will be wrapped around to the other end of RAM and continue.

MX IMPLEMENTATION

Column Mirroring (MX) is implemented by selecting either (CA) or (240-CA) as the RAM column address. Changing MX affects the data written to the RAM.

Since MX has no effect of the data already stored in RAM, changing MX does not have immediate effect on the displayed pattern. To refresh the

display, refresh the data stored in RAM after setting MX.

ROW SCANNING

For each field, the scanning starts at R1 through R_m, where *m* may be 96, or 128, depends on the setting of MR.

Row electrode scanning orders are not affected by Start Line (SL) or Mirror Y (MY, LC[3]). When MY is 0, the effect of SL having a value *K* is to change the mapping of R0 to the *K*-th bit slice of data stored in display RAM. Visually, SL having a non-zero value is equivalent to scrolling LCD display by SL rows.

RAM ADDRESS GENERATION

The mapping of the data store in the display SRAM and the scanning electrodes can be obtained by combining the fixed R_m scanning sequence and the following RAM address generation formula.

During the display operation, the RAM line address generation can be mathematically represented as following:

For the 1st line period of each field
 $Line = SL$

Otherwise
 $Line = Mod(Line+1, 128)$

Where Mod is the modular operator, and *Line* is the bit slice line address of RAM to be outputted to column drivers. Line 0 corresponds to the first bit-slice of data in RAM.

The above *Line* generation formula produce the "loop around" effect as it effectively resets *Line* to 0 when *Line+1* reaches 128.

MY IMPLEMENTATION

Row Mirroring (MY) is implemented by reversing the mapping order between row electrodes and RAM, i.e. the mathematical address generation formula becomes:

For the 1st line period of each field
 $Line = Mod(SL + MUX-2, 128)$
 where MUX = 96, or 128

Otherwise
 $Line = Mod(Line-1 , 128)$

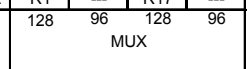
Visually, the effect of MY is equivalent to flipping the display upside down. The data stored in display RAM is not affected by MY.

MSF		Line Addresss
0	1	
D0	D7	00H
D1	D6	01H
D2	D5	02H
D3	D4	03H
D4	D3	04H
D5	D2	05H
D6	D1	06H
D7	D0	07H
D0	D7	08H
D1	D6	09H
D2	D5	0AH
D3	D4	0BH
D4	D3	0CH
D5	D2	0DH
D6	D1	0EH
D7	D0	0FH
D0	D7	10H
D1	D6	11H
D2	D5	12H
D3	D4	13H
D4	D3	14H
D5	D2	15H
D6	D1	16H
D7	D0	17H
D0	D7	18H
D1	D6	19H
D2	D5	1AH
D3	D4	1BH
D4	D3	1CH
D5	D2	1DH
D6	D1	1EH
D7	D0	1FH
D0	D7	28H
D1	D6	29H
D2	D5	2AH
D3	D4	2BH
D4	D3	2CH
D5	D2	2DH
D6	D1	2EH
D7	D0	2FH
D0	D7	30H
D1	D6	31H
D2	D5	32H
D3	D4	33H
D4	D3	34H
D5	D2	35H
D6	D1	36H
D7	D0	37H
D0	D7	38H
D1	D6	39H
D2	D5	3AH
D3	D4	3BH
D4	D3	3CH
D5	D2	3DH
D6	D1	3EH
D7	D0	3FH

								Page 0															
								Page 1															
								Page 2															
								Page 3															
								Page 13															
								Page 14															
								Page 15															

MY=0		MY=1			
SL=0	SL=16	SL=0	SL=0	SL=16	SL=16
R1	R113	R128	R96	R16	---
R2	R114	R127	R95	R15	---
R3	R115	R126	R94	R14	---
R4	R116	R125	R93	R13	---
R5	R117	R124	R92	R12	---
R6	R118	R123	R91	R11	---
R7	R119	R122	R90	R10	---
R8	R120	R121	R89	R9	---
R9	R121	R120	R88	R8	---
R10	R122	R119	R87	R7	---
R11	R123	R118	R86	R6	---
R12	R124	R117	R85	R5	---
R13	R125	R116	R84	R4	---
R14	R126	R115	R83	R3	---
R15	R127	R114	R82	R2	---
R16	R128	R113	R81	R1	---
R17	R1	R112	R80	R128	---
R18	R2	R111	R79	R127	---
R19	R3	R110	R78	R126	---
R20	R4	R109	R77	R125	---
R21	R5	R108	R76	R124	---
R22	R6	R107	R75	R123	---
R23	R7	R106	R74	R122	---
R24	R8	R105	R73	R121	---
R25	R9	R104	R72	R120	R96
R26	R10	R103	R71	R119	R95
R27	R11	R102	R70	R118	R94
R28	R12	R101	R69	R117	R93
R29	R13	R100	R68	R116	R92
R30	R14	R99	R67	R115	R91
R31	R15	R98	R66	R114	R90
R32	R16	R97	R65	R113	R89
R105	R89	R24	---	R40	R8
R106	R90	R23	---	R39	R7
R107	R91	R22	---	R38	R6
R108	R93	R21	---	R37	R5
R109	R93	R20	---	R36	R4
R110	R94	R19	---	R35	R3
R111	R95	R18	---	R34	R2
R112	R96	R17	---	R33	R1
R113	R97	R16	---	R32	---
R114	R98	R15	---	R31	---
R115	R99	R14	---	R30	---
R116	R100	R13	---	R29	---
R117	R101	R12	---	R28	---
R118	R102	R11	---	R27	---
R19	R103	R10	---	R26	---
R120	R104	R9	---	R25	---
R121	R105	R8	---	R24	---
R122	R106	R7	---	R23	---
R123	R107	R6	---	R22	---
R124	R108	R5	---	R21	---
R125	R109	R4	---	R20	---
R126	R110	R3	---	R19	---
R127	R111	R2	---	R18	---
R128	R112	R1	---	R17	---

MX	0	C240	C1	C239	C2	C238	C3	C237	C4	C236	C5	C235	C6	C234	C7	C233	C8	C236	C5	C237	C4	C238	C3	C239	C2	C240	C1
	1																										



RESET & POWER MANAGEMENT

TYPES OF RESET

UC1608 has two different types of Reset: *Power-ON-Reset* and *System-Reset*.

Power-ON-Reset is performed right after V_{DD1} is connected to power. *Power-On-Reset* will first wait for about 12mS, depending on the time required for V_{DD} to stabilize, and then trigger the *System Reset*.

System Reset can also be activated by software command or by connecting RST pin to ground.

In the following discussions, Reset means *System Reset*.

RESET STATUS

When UC1608 enters RESET sequence:

- All non-pin configurable control registers will be reset to their default values.
- All pin configurable control registers will be reset according to their configuration pins.
- Operation mode will be “Reset”
- System Status bits RS and BZ will stay as “1” until the Reset process is completed.

Refer to Control Registers for details of control flags and their default values. Refer to Pin Description for configuration pin definitions.

When RS=1, only status read command is processed by UC1608. All other commands are ignored.

Once entered Reset mode, all control registers will be reset to their default values and capacitors will be discharged. In general it is necessary to set up control registers before transition out of the Reset mode.

OPERATION MODES

UC1608 has three operating modes (OM): Reset, Normal, Sleep.

Mode	Reset	Sleep	Normal
OM	00	10	11
Host Interface	Active	Active	Active
Clock	OFF	OFF	ON
LCD Drivers	OFF	OFF	ON
Charge Pump	OFF	OFF	ON
Draining Circuit	ON	OFF	OFF

Table 11: Operating Modes

CHANGING OPERATION MODE

Two commands will initiate OM transitions: *Set Display Enable*, and *System Reset*.

Action	Mode	OM
Set Driver Enable to “000”	Sleep	10
Set Driver Enable “ON”	Normal	11
Reset command RST_ pin pulled “L” Power ON reset	Reset	00

Table 12: OM changes

When DC[2] is modified by *Set Display Enable*, OM will be updated automatically. There is no other action required to enter power saving mode.

For maximum energy utilization, Sleep mode is designed to retain charges stored in external capacitors C_{B0} , C_{B1} , C_{B2} , C_{B3} and C_{LCD} . To drain these capacitors, use Reset command to activate the on-chip draining circuit.

OM changes are synchronized with the edges of UC1608 internal clock. To ensure consistent system states, wait at least 10uS after *System Reset* or *Set Display Enable* command.

EXITING POWER SAVE MODES

UC1608 contains internal logic to check whether V_{LCD} and V_{BIAS} is ready before releasing row and column drivers from their OFF states. When exiting Sleep Mode and Reset Mode, column and row drivers will not be activated until UC1608 internal voltage sources are restored to their proper values.

Although explicit wait before turning on the display (Set DC[2] to non-zero) is not required, operation sequence wise, it is generally a good practice to do this as the last step when exiting from Sleep or Reset mode.

POWER-UP SEQUENCE

UC1608 power-up sequence is simplified by built-in “Power Ready” flags and by the automatic invocation of *System-Reset* command after *Power-ON-Reset*. System programmer are only required to wait ~30 ms before starting to issue commands to UC1608. No additional commands or waits are required between enabling of the charge pump, turning on the display drivers, writing to RAM or any other commands.

POWER-DOWN SEQUENCE

To prevent the charge stored in capacitors C_{BX+} , C_{BX-} , and C_{LCD} from damaging the LCD when

V_{DD} is switched off, use Reset mode to enable the built-in charge draining circuit to discharge these external capacitors.

UC1608 draining resistance is 1K for both V_{LCD} and V_{B+} . It is recommended to wait $3 \times RC$ for V_{LCD} and $1.5 \times RC$ for V_{B+} before allowing V_{DD} to drop below 2V. For example, if C_{LCD} is 1 μ F, then the draining time required for V_{LCD} is 3~5mS.

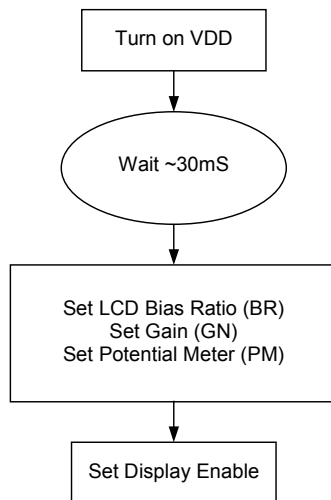


Figure 12: Reference Power-up Sequence

UC1608 will *not* drain V_{LCD} when internal V_{LCD} is not used. System designer should take care to make sure external V_{LCD} source is properly drained off before turning off VDD.

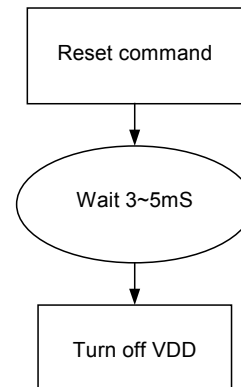


Figure 13: Reference Power-Down Sequence

SAMPLE COMMAND SEQUENCES

The following table are host interface examples for various UC1608 operations.

Step sequences starting with the same number (such as 2a, 2b, 2c, ...) can be rearranged without affecting the result. Some optional steps have mutual dependencies. Such mutually-dependent optional steps need to be elected or skipped together as a group.

C/D The type of the interface cycle. Depending on the interface type (parallel or serial).

W/R The direction of data flow of the cycle. It can be either Write (0) or Read (1).

BZ, OM The status of these flags “during” the operation of the command.

(Opt.) Optional item.

POWER-UP SEQUENCE

The only “required” command to initialize UC1608 is *Set Display ON*. However, many other commands (such as *Set APO = 0/1*, *Set LCD Mapping*) and any of the NOP bit patterns can be used for maximum software compatibility with other industry leading LCD controller-drivers.

Example 1: Use System Reset command.

#	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Operation	OM	BZ	Comments
	—	—	—	—	—	—	—	—	—	—	Power-On reset. V _{DD} powering up. Wait ~30mS for V _{DD} to become steady.	—	1	(Recommended) Use “Read Status” to make sure BZ flag is 0 before issuing any other command.
	—	—	—	—	—	—	—	—	—	—	Automatic System Reset.	—	1	
	0	1	D	D	D	D	—	—	—	—	(Opt.) Read Status	00	0	
	0	0	1	0	1	0	1	0	0	0	(Opt.) System Reset	00	0	Recommended.
	0	0	1	1	1	0	1	0	#	#	(Opt.) Set Bias Ratio	00	0	
	0	0	0	0	1	0	0	#	#	#	(Opt.) Set Gain	00	0	
	0	0	1	0	0	0	0	0	0	1	(Opt.) Set PM	00	0	
	—	—	—	—	#	#	#	#	#	#				
	0	0	0	0	1	0	1	#	#	#	(Opt.) Set Power Control	00	0	If external V _{LCD} is selected, activate the source here.
	0	0	1	0	1	0	1	1	1	1	Set Display ON	11	0	

Note1: It is recommended to wait at least 20mS after power on. Otherwise commands issued to UC1608 may be overlooked because the chip is still in the power up process.

Note2: Example 1 does not require to use of RST pin and therefore is more appropriate for applications where compact connector size is critical.

Example 2: Use RST pin.

#	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Operation	OM	BZ	Comments
	-	-	-	-	-	-	-	-	-	-	Hold RST pin to "L" until the external power is stable.	—	1	
	0	1	D	D	D	D	-	-	-	-	(Opt.) Read Status	00	0	Recommended
	0	0	1	1	1	0	0	0	1	0	(Opt.) System Reset	00	0	Recommended
	0	0	1	1	1	0	1	0	#	#	(Opt.) Set Bias Ratio	00	0	
	0	0	0	0	1	0	0	#	#	#	(Opt.) Set Gain	00	0	
	0	0	1	0	0	0	0	0	0	1	(Opt.) Set PM	00	0	
	-	-	-	-	#	#	#	#	#	#				
	0	0	0	0	1	0	1	#	#	#	(Opt.) Set Power Control	00	0	If external V_{LCD} is selected, activate the source here.
	0	0	1	0	1	0	1	1	1	1	Set Display ON	11	0	

POWER-DOWN SEQUENCES

Option 1: Use System Reset command.

#	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Operation	OM	BZ	Comments
	0	0	1	1	1	0	0	0	1	0	System Reset	00	1	
	-	-	-	-	-	-	-	-	-	-	(Wait 3~5mS)	00	0	Draining C_{LCD} , C_B
	-	-	-	-	-	-	-	-	-	-	Turn off V_{DD}	00	0	

Note: Option 1 does not require the use of RST pin and therefore is more appropriate for applications where compact connector size is critical.

Option 2: Use RST pin.

#	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Operation	OM	BZ	Comments
	-	-	-	-	-	-	-	-	-	-	Hold RST to "L", wait 3~5mS	00	1	Draining C_{LCD} , C_B
	-	-	-	-	-	-	-	-	-	-	Turn off V_{DD}	00	0	

PREPARE TO ACCESS DATA RAM

Address control (register AC) flags and some LCD to SRAM mapping (register LC) flags affect how data is stored into the display buffer SRAM => Make proper adjustment to these two registers before writing data to UC1608 display buffer SRAM.

These commands can be performed under any operating mode (OM).

#	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Operation	OM	BZ	Comments
	0	0	1	0	0	0	1	#	#	#	(Opt.) Set Address Control	-	0	
	0	0	1	1	0	0	#	#	0	#	(Opt.) Set/clear LCD Mapping control flags.	-	0	

DATA RAM ACCESS: WRITE

These sequence can be performed in parallel 8-bit. These commands can be performed under any operating mode (OM).

#	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Operation	OM	BZ	Comments
1	0	0	1	0	1	1	#	#	#	#	Set Page Address	-	0	
2	0	0	0	0	0	1	#	#	#	#	Set Column Address MSB	-	0	
3	0	0	0	0	0	0	#	#	#	#	Set Column Address LSB	-	0	
4	1	0	#	#	#	#	#	#	#	#	Write Display Data (repeat as appropriate)	-	0	
5											(Return to 1 as necessary, repeat until complete)	-	0	

DATA RAM ACCESS: READ

For parallel interface modes, a dummy Read cycle is required when a Read Data command follows immediately after a Write cycle (either Write Data or Write Control).

#	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Operation	OM	BZ	Comments
1	X	0	1	0	1	1	#	#	#	#	Write cycle (either data or control)	-	0	For example: Commands setting PA and/or CA.
2	1	1	-	-	-	-	-	-	-	-	Dummy Read cycle	-	0	
3	1	1	#	#	#	#	#	#	#	#	Read Display Data (repeat as appropriate)	-	0	

DATA RAM ACCESS: CURSOR UPDATE

Cursor can be used to support many flexible graphics user interface designs. Blinking cursor requires frequent update to a limited set of pixels. UC1608 Cursor update mode is designed to facilitate such frequent data RAM updates.

Under Cursor Update mode, both the automatic wrap around (CA reset to 0, PA increment or decrement) and CA increment on Read are disabled temporarily. These two features allow system designer to minimize the need to update CA and PA registers and allows on-chip RAM to be used in Read-Modify-Write style operations.

EXAMPLE 1: CURSOR UPDATE WITH READ-MODIFY-WRITE

#	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Operation	OM	BZ	Comments
1	0	0	1	1	1	0	0	0	0	0	Set Cursor-Update mode and set CR=CA	-	0	CR tracks where CA should be restored later
2	1	1	-	-	-	-	-	-	-	-	Dummy Read cycle	-	0	CA unchanged
	1	1	#	#	#	#	#	#	#	#	Read Display Data			
3	1	0	#	#	#	#	#	#	#	#	Write Display Data	-	0	CA will increment, but will not wrap around
											(Return to 2 and repeat until the cursor is updated)	-	0	
4	0	0	1	1	1	0	1	1	1	0	Clear Cursor Update Mode	-	0	Set CA=CR
											Return to 1 for next cursor update cycle or continue	-	0	

EXAMPLE 2: CURSOR UPDATE WITHOUT READ

#	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Operation	OM	BZ	Comments
1	0	0	1	1	1	0	1	1	1	1	Set Cursor-Update mode and set CR=CA	-	0	CR remembers where CA should be restored later
2	1	0	#	#	#	#	#	#	#	#	Write Display Data	-	0	CA will increment but will not wrap around
3											(Return to 2 and repeat until the cursor is updated)	-	0	
4	0	0	1	1	1	0	1	1	1	0	Clear Cursor Update Mode	-	0	Set CA=CR
											Return to 1 for next cursor update cycle or continue	-	0	

ENABLE DISPLAY

#	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Operation	OM	BZ	Comments
	0	0	0	1	#	#	#	#	#	#	(Opt.) Set Start Line	-	0	
	0	0	1	0	1	0	0	1	0	#	(Opt.) Set All-Pixel-ON	-	0	
	0	0	1	0	1	0	0	1	1	#	(Opt.) Set Inverse Mode.	-	0	
	0	0	1	0	1	0	1	1	1	1	Set Display ON	11	0	

Note: The order of these steps is not critical. However, for the smoothness of display effect, the above sequence is recommended.

ABSOLUTE MAXIMUM RATINGS

In accordance with IEC134, note 1, 2 and 3.

Symbol	Parameter	Min.	Max.	Unit
V_{DD1}	Logic Supply voltage	-0.3	+4.0	V
V_{DD2}	LCD Generator Supply voltage	-0.3	+4.0	V
V_{DD3}	Analog Circuit Supply voltage	-0.3	+4.0	V
V_{LCD}	LCD Generated voltage	-0.3	+18.0	V
V_{IN} / V_{OUT}	Any input/output	-0.3	$V_{DD} + 0.3$	V
T_{OPR}	Operating temperature range	-30	+85	°C
T_{STR}	Storage temperature	-50	+100	°C
T_J	Junction temperature		+120	°C
P_{IC}	Total power dissipation		200	mW

Notes

1. V_{DD} based on $V_{SS} = 0V$
2. Stress above values listed may cause permanent damages to the device.

SPECIFICATIONS

DC CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD1}	Digital Supply voltage		2.4		4.0	V
V_{DD2}	Supply for V_{LCD} generation		2.4		4.0	V
V_{LCD}	LCD Driving Voltage				17.0	V
V_{B0}	LCD Bias Voltage				1.6V	V
V_{IL}	Input logic LOW					V
V_{IH}	Input logic HIGH					V
V_{OL}	Output logic LOW					V
V_{OH}	Output logic HIGH					V
I_{IL}	Input leakage current					μ A
I_{OZ}	Output leakage current					μ A
$R_{0(col.)}$	Column output impedance	$V_{LCD} = 15V$		2.0	2.7	$k\Omega$
$R_{0(row)}$	Row output impedance	$V_{LCD} = 15V$		2.0	2.7	$k\Omega$
f_{CLK}	Internal clock frequency		275	335	400	kHz

AC CHARACTERISTICS

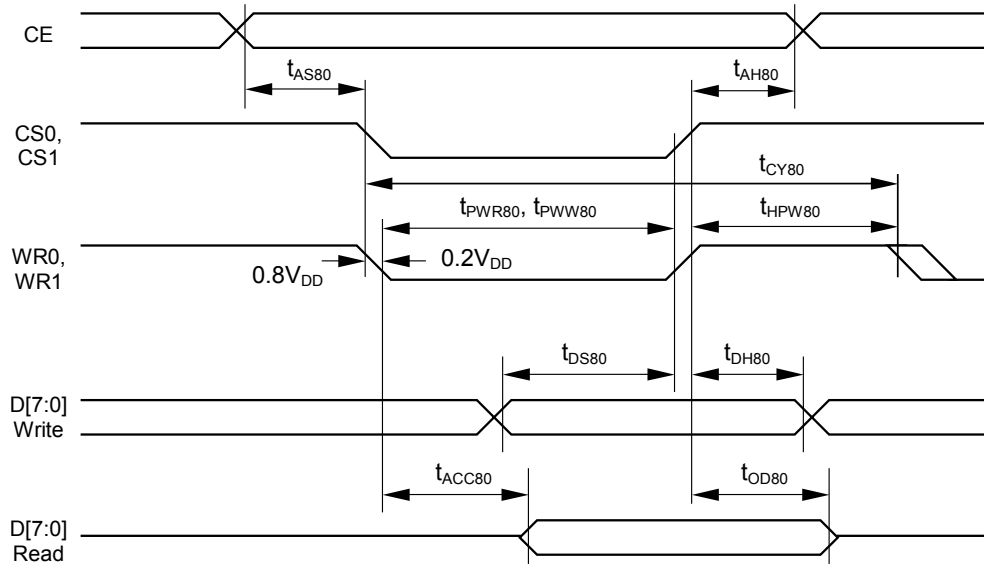


Figure 21: Parallel Bus Timing Characteristics (for 8080 MCU)

(VDD=2.4V to 3.0V, Ta= -30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t _{AS80}	CD	Address setup time		20	-	ns
t _{AH80}	CD	Address hold time		40	-	ns
t _{CY80}		System cycle time		100	-	ns
t _{PWR80}	WR1	Pulse width (read)		45	-	ns
t _{PWW80}	WR0	Pulse width (write)		45	-	ns
t _{HPW80}	WR0, WR1	High pulse width		40	-	ns
t _{DS80}	D0~D7	Data setup time		30	-	ns
t _{DH80}	D0~D7	Data hold time		10	-	ns
t _{ACC80}		Read access time	C _L = 100pF	-	50	ns
t _{OD80}		Output disable time		10	50	ns

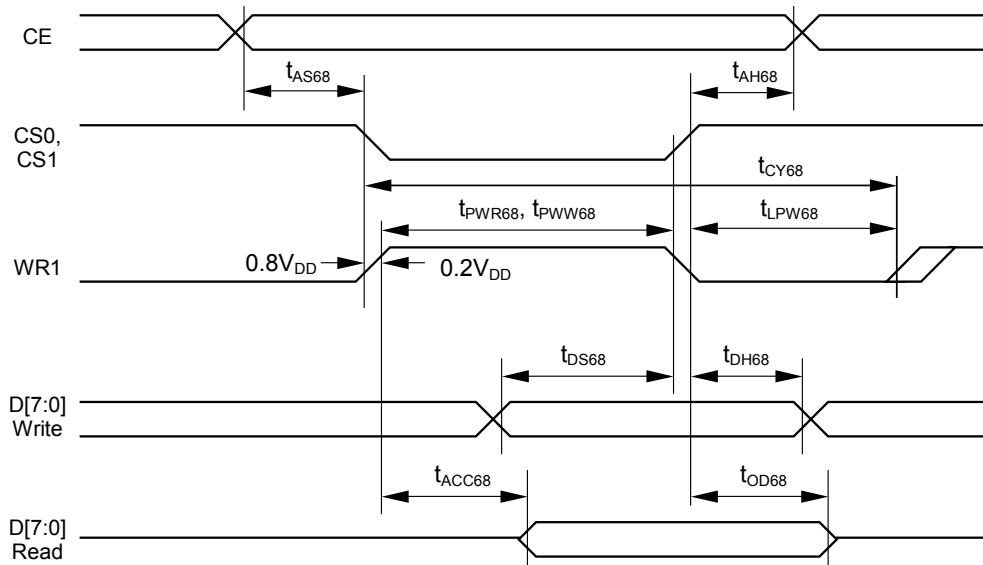


Figure 22: Parallel Bus Timing Characteristics (for 6800 MCU)

(VDD=2.4V to 3.0V, Ta= -30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68}	CD	Address setup time		20	–	ns
t_{AH68}		Address hold time		40	–	ns
T_{CY68}		System cycle time		100	–	ns
t_{PWR68}	WR1	Pulse width (read)		45	–	ns
t_{PWW68}		Pulse width (write)		45	–	ns
t_{LPW68}		Low pulse width		40	–	ns
t_{DS68}	D0~D7	Data setup time		30	–	ns
t_{DH68}		Data hold time		10	–	ns
t_{ACC68}		Read access time	$C_L = 100\text{pF}$	–	50	ns
t_{OD68}		Output disable time		10	50	ns

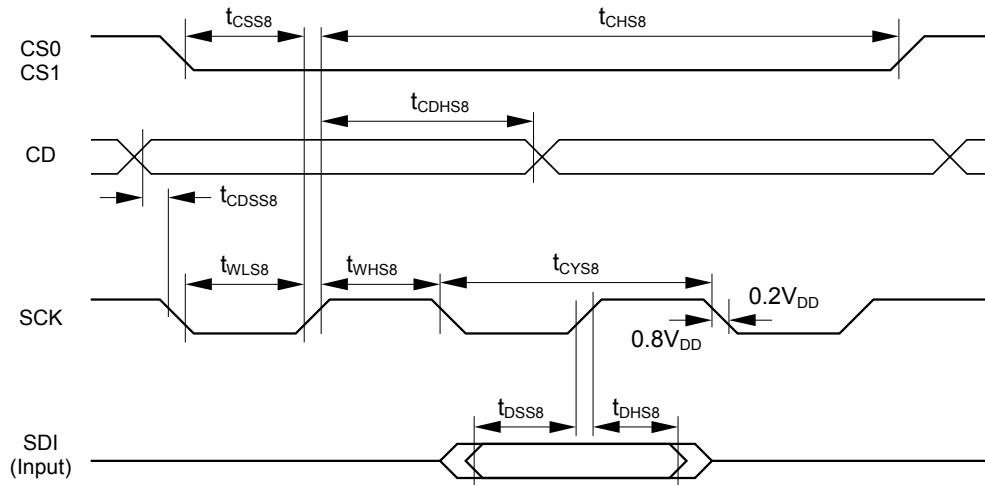


Figure 23: Serial Bus (8-bit mode) Timing Characteristics

(VDD=2.4V to 3.0V, Ta= -30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{CSS8}	CS	CS setup time		50	-	ns
t_{CHS8}	CS	CS hold time		50	-	ns
t_{CDSS8}	CD	CD setup time		20	-	ns
t_{CDHS8}	CD	CD hold time		40	-	ns
t_{CYS8}	SCK	SCK clock cycle		100	-	ns
t_{WHS8}	SCK	SCK high width		45	-	ns
t_{WLS8}	SCK	SCK low width		45	-	ns
t_{DSS8}	SDI	Data setup time		30	-	ns
t_{DHS8}	SDI	Data hold time		10	-	ns

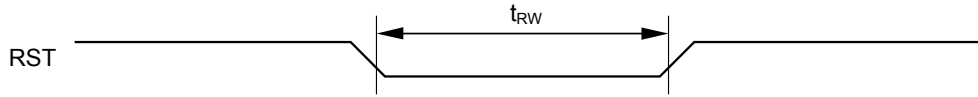


Figure 25: Reset Characteristics

(VDD=2.4V to 3.0V, Ta= -30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{RW}	RST	Reset low pulse width		100	–	ns

UC1608 PHYSICAL DIMENSION

CHIP SIZE
12.5369x 1.208 μm
AU BUMP HEIGHT:
17 $\mu\text{m} \pm 1 \mu\text{m}$ (within die)
AU BUMP PITCH:
50 μm
AU BUMP SIZE:
94 x 32 μm
DUMMY BUMP SIZE:
94 x 57 μm
PAD COORDINATES:
Pad center
PAD ORIGIN:
Chip center

